ABSTRACT OF THE DISCLOSURE

A master-slave-type scanning flip-flop circuit is capable of operating at a higher speed by reducing a load capacity of a clock controller. The master-slave-type scanning flip-flop circuit is used to test a semiconductor integrated circuit device, and has a master latch and a slave latch each for temporarily holding an input signal, a first scan controller, a clock controller, and a second scan controller. The first scan controller receives an output signal from the master latch and outputs the received output signal in synchronism with a scan clock which is a clock for testing the semiconductor integrated circuit device, when the semiconductor integrated circuit device is tested. The clock controller receives an output signal from the first scan controller and outputs the received output signal to the slave unit in synchronism with a predetermined clock when in a normal mode of operation. The second scan controller has an input terminal connected to an output terminal of the first scan controller, and outputs a scan-out signal corresponding to a scan-in signal which is an input signal for testing the semiconductor integrated circuit device, in synchronism with the scan clock when the semiconductor integrated circuit device is tested.